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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/672,750
Filing Date: September 25, 2003
Appellant(s): COBBLEY ET AL.

Robert A. Manware
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/21/06 appealing from the Office action mailed 2/15/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US006503776B2	**Pai et al**	**7-2003**
US006753206B2	**Huang et al**	**6-2004**
US006627477B1	**Hakey et al**	**9-2003**

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 35, 37-39, 45, 47-49, 63, 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pai (US006503776B2) in view of Huang (US006753206B2).

Pai teaches the device of claims 38-39, 48-49, and 66 as except for the stack being a shingle stack (defined in the instant specification where the die centers are not aligned) and for the at least two die being electrically functional.

Regarding claim 35, An integrated circuit comprising a stack comprising at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**,

each of the semiconductor die being coupled together by a first adhesive, the first adhesive **(166)** being curable at a first temperature; and

a substrate coupled **(substrate 120 coupled to stack through chip 110 and adhesive 162)** to one of the at least two semiconductor die by a second adhesive **(112)**, the second adhesive being curable at a second temperature lower than the first temperature; **(it is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two semiconductor die is functional **(Pai teaches a dummy die, the dummy die serving a function, thus being functional.)**

Regarding the limitation where the at least two die are electrical functional, Pai teaches one of the die is a dummy die, but of the same material as the electrically functional die. Thus by forming a wire, the dummy die could then serve an electrical function. Huang forms a stack similar to that of Pai, but teaches a stack where all die are "electrically" functional. It would be obvious to one skilled in the art to modify Pai by using an electrically functional die in the stack as taught by Huang.

Regarding claim 37. The integrated circuit, as set forth in claim 35, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die **(See figure 10)**.

Regarding claim 38. An integrated circuit comprising:

a stack comprising at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the semiconductor die being coupled together by a first adhesive, the first adhesive **(166)** being curable at a first temperature; and

a substrate coupled **(substrate 120 coupled to stack through chip 110 and adhesive 162)** to one of the at least two semiconductor die by a second adhesive **(112)**, the second adhesive being curable at a second temperature lower than the first temperature; **(It is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack **(Huang teaches a conventional stack (prior art) and a shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47)) Further, it is noted that the instant application teaches a "conventional stack" also**.

Regarding claim 39. The integrated circuit, as set forth in claim 35, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

Regarding claim 45. An integrated circuit comprising a stack of at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the die being coupled to an adjacent die in the stack **(110)** by a respective layer of adhesive **(162)** prior to the stack being coupled to a packaging substrate. **(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)
wherein each die in the stack of at least two semiconductor die is functional **(Pai teaches a dummy die, the dummy die serving a function, thus being functional.)**

Regarding the limitation where the at least two die are electrical functional, Pai teaches one of the die is a dummy die, but of the same material as the electrically functional die. Thus by forming a wire, the dummy die could then serve an electrical function. Huang forms a stack similar to that of Pai, but teaches a stack where all die are "electrically" functional. It would be obvious to one skilled in the art to modify Pai by using an electrically functional die in the stack as taught by Huang.

Regarding claim 48. An integrated circuit comprising a stack of at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the die being coupled to an adjacent die in the stack **(110)** by a respective layer of adhesive **(162)** prior to the stack being coupled to a packaging substrate; **(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack **(Huang teaches a conventional stack (prior art) and a shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47))**.

Regarding claim 47. The integrated circuit, as set forth in claim 45, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die **(See figure 10)**.

Regarding claim 49. The integrated circuit, as set forth in claim 45, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

Regarding claim 63. An integrate circuit package comprising:

a substrate **(120)**; and

a die stack coupled to the substrate **(Figure 10)**, wherein the die stack comprises at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)** coupled together and wherein the dies stack is formed prior to being coupled to the substrate;

(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two semiconductor die is functional **(Pai teaches a dummy die, the dummy die serving a function, thus being functional.)**

Regarding the limitation where the at least two die are electrical functional, Pai teaches one of the die is a dummy die, but of the same material as the electrically functional die. Thus by forming a wire, the dummy die could then serve an electrical function. Huang forms a stack similar to that of Pai, but teaches a stack where all die are "electrically" functional. It would be obvious to one skilled in the art to modify Pai by using an electrically functional die in the stack as taught by Huang.

Regarding claim 65. The integrated circuit package, as set forth in claim 63, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die **(See figure 10)**.

Regarding claim 67. The integrated circuit package, as set forth in claim 63, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

Regarding claim 66. An integrate circuit package comprising:

a substrate **(120)**; and

a die stack coupled to the substrate **(Figure 10)**, wherein the die stack comprises at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)** coupled together and wherein the dies stack is formed prior to being coupled to the substrate;

(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack **(Huang teaches a conventional stack (prior art) and a**

shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47)).

It would be obvious to one skilled in the requisite art at the time of the invention would modify Pai by including an electrically functional die and a shingle stack as taught by Huang to be an improvement with chips of varied sizes **(Huang teaches a conventional stack (prior art) and a shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47)).**

3. Claims 68-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pai (US006503776B2) in view of Hakey (US006627477B1).

Pai teaches the device of claims 68-70 as except for explicitly teaching that each die in the stack may successively thinner than the previous one.

Claim 68. An integrated circuit comprising:

a stack comprising at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the semiconductor die being coupled together by a first adhesive, the first adhesive **(166)** being curable at a first temperature; and

a substrate coupled **(substrate 120 coupled to stack through chip 110 and adhesive 162)** to one of the at least two semiconductor die by a second adhesive **(112)**, the second adhesive being curable at a second temperature lower than the first temperature; **(it is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two die is successively thinner than the previous die (**Pai teaches combining chips of processor, memory and associated logic into a single package (column 1 lines 17-19). Although not teaching that these chips may have a different thickness from each other, one skilled in the requisite art would know this. Hakey does not stack the die, but also connects die of logic chips and memory chips and teaches that these die have different thicknesses (column 2 lines 34-40), thus confirming that one would know that the chips of Pai could be of a different thickness from each other. In a stack of two die of different thicknesses, it is inherent that one die be successively thinner than the previous die).**

Claim 69. An integrated circuit comprising a stack of at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the die being coupled to an adjacent die in the stack **(110)** by a respective layer of adhesive

(162) prior to the stack being coupled to a packaging substrate; **(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two die is successively thinner than the previous die (**Pai teaches combining chips of processor, memory and associated logic into a single package (column 1 lines 17-19). Although not teaching that these chips may have a different thickness from each other, one skilled in the requisite art would know this. Hakey does not stack the die, but also connects die of logic chips and memory chips and teaches that these die have different thicknesses (column 2 lines 34-40), thus confirming that one would know that the chips of Pai could be of a different thickness from each other. In a stack of two die of different thicknesses, it is inherent that one die be successively thinner than the previous die)**.

Claim 70. An integrate circuit package comprising:

a substrate **(120)**; and

a die stack coupled to the substrate **(Figure 10)**, wherein the die stack comprises at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)** coupled together and wherein the dies stack is formed prior to being coupled to the substrate;

(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack is successively thinner than the previous die (**Pai teaches combining chips of processor, memory and associated logic into a single package (column 1 lines 17-19). Although not teaching that these chips may have a different thickness from each other, one skilled in the requisite art would know this. Hakey does not stack the die, but also connects die of logic chips and memory chips and teaches that these die have different thicknesses (column 2 lines 34-40), thus confirming that one would know that the chips of Pai could be of a different thickness from each other. In a stack of two die of different thicknesses, it is inherent that one die be successively thinner than the previous die).**

It would be obvious to one skilled in the requisite art at the time of the invention to modify Pai to include chips having a different thickness as suggested by Pai's description of the chips, Hakey teaching that the chips listed by Pai have different thicknesses.

(10) Response to Argument

A. Ground of rejection No. 1

1. The appellant states case law regarding prima facie obviousness and hindsight construction, but makes no argument (here) as to how the examiner failed to meet the criteria.

2. The appellant argues that the rejection fails to establish a prima facie case of obviousness in regard to independent claims 35, 45, and 63. Specifically, the appellant argues this toward the limitation that "each die in the stack be electrically functional".

First, it is important to define "electrically functional". The term does not appear in the specification. This in itself allows for a broad interpretation. The appellant (page 4 of the instant brief) points to the specification (page 12 lines 10-12, page 17 line 13, and page 18, line 3 for support of "electrically functional". However, page 12 lines 10-12 merely recite, "the die may be tested to ensure that all die in the stack are functional". The dummy die of Pai would read on this. Page 17 line 13 recites, "Further the die stack can be electronically tested prior to attachment to a substrate". Pai also reads on this. Testing the die **stack** electrically does not mean all die must be electronically functional (working active devices). It only means the stack as a whole is tested. Not only does this recitation allow for dummy die, but even if the dummy die of Pai were electronically tested and found to have no active devices, it qualifies as a die by this teaching. Page 18, line 3, recites, "after the testing, the die stacks may be attached..." As above this is testing the die stack as a whole, not individual die, and even if the dummy die of Pai

were electronically tested and found to have no active devices, it qualifies as a die by this teaching. Also note that the claims do not have any limitations as to testing of the die or die stacks.

Thus if we define "electrically functional" in light of the specification as pointed to by the appellant, the dummy die of Pai qualifies as its electrical function is to provide clearance for wiring (Pai column 1 lines 66-67) between two other active chips (110 and 130).

If a narrower interpretation of "electrically functional" is read into the claim language, the secondary reference of Huang is used to modify Pai, with Huang teaching that all die are electrically active. As Pai teaches the dummy die to be of the same material as the other die, a substitute of an active die for the dummy die (as suggested by Huang) would be an easy substitution, without altering the function of Pai as the die would still create wiring space.

The appellant argues that Pai does not attach wiring to the dummy chip because the dummy chip is not employed in the device operation and the die is not electrically functional. As recited above, the dummy die of Pai is electrically functional, its electrical function being the creation of wiring space. Further, this argument merely attacks the single reference of Pai without regard to Huang. If "electrically functional" necessitates "active devices", Huang teaches this.

Regarding claim 35, the appellant argues that one of the disadvantages of prior stacking techniques is that damaged die may be unknowingly incorporated into a stacked package and that in accordance with embodiments of the present invention, each of the die are tested to ensure that all die are functional. As above, we would be confronted with defining "functional" to determine whether the dummy die of Pai is "functional". However, the limitations regarding testing are not in the instant claims, thus the argument is moot. The argument toward "the die stack can be electrically tested prior to attachment to a substrate" does not mean all die are electrically active, but that the stack itself is tested. This would allow for a dummy die or modification (as suggested by Huang) for an active die. Further, there are no limitations as to this teaching in the instant specification.

The appellant argues that it is clear that an "electrically functional" die refers to the die being capable of performing its electronic function. If by "its electronic function" it is meant active devices, this is not clear from the specification. Nowhere in the instant specification does electrically functional appear, nor does the instant specification define what a function is. The dummy die serves its electronic function by allowing for electrical wiring space. Also, as above, this argument attacks the references piecemeal, rather than as a whole. Even if the dummy die of Pai does not read on "electrically functional", in light of Huang's suggestion, one of ordinary skill in the art would know that the dummy die could be replaced by an active device die.

The appellant repeats the argument that Pai teaches that the dummy die does not require wiring. As recited above, this does not mean that the dummy die of Pai does not serve an electric function, nor that substitution in light of Huang for an active device die is not obvious, nor does this argument attack the rejection as a whole, but merely a piecemeal attack on an individual reference.

The appellant aggress with the examiner that the dummy die does have a function, but that those skilled in the art would not interpret the die as "electrically functional". This argument is an assumption of how one would interpret the claim language. As the term "electrically functional" does not appear in the instant specification and therefore is not clearly defined, the broadest interpretation must be applied. As above, this is a piecemeal attack on an individual reference.

In regard to Huang, the appellant argues that Huang merely discloses coupling two chips in a lead frame and this differs from packaging incorporating a chip coupled to a substrate. However, they are related art, both dealing with coupling die. Further, Huang was used to suggest that Pai substitute an active device die for a dummy die. The appellant points to its own specification regarding mismatches in thermal coefficients to support this. However, this would not preclude one from substituting an active device die (per Huang) for the dummy die. In fact, Pai teaches the dummy die be of the same material, thus a thermal expansion mismatch is avoided. Further, an active die of Pai of

the same material (without wiring) would be within Pai's own teaching. Only wiring need be added.

The appellants argue that there is no motivation to substitute the dummy die for an active device die of Huang. The examiner disagrees, as motivation was provided, the substitution being obvious and an improvement as to incorporating die of different sizes.

The appellants argue regarding the examiner's statements (Response to Arguments, Final rejection) and that the reference to Huang (by appellants) was made to show that the dummy chip of Pai is simply a feature and the appellants argue about the dummy chip not being wired nor incorporated into the operation. The examiner responded to such arguments above.

The appellants argue that Pai teaches away from incorporating electrically functional die. The examiner disagrees because as above, the dummy die has an electrical function. Further, as it spaces die for wiring, the only need for an electrically active die is wiring. As the die is of the same material, this suggests an active device die as in the die below and above. There are no limitations that the die need be wired; only that it serves an electric function, undefined by the instant specification.

The appellants argue that they are unaware of how one skilled in the art could modify the package of Pai in view of Huang. The examiner asserts that if the dummy die of Pai

does not serve an electric function, then an active device die could be substituted as suggested by Huang (all die have devices.).

The appellants argue against inappropriate official notice taken by the examiner (page 13 of the final office action). Page 13 is part of the examiner's response to applicant's arguments, is not part of the rejection, and no official notice was taken.

The appellants argue that for the reasons set forth above, that claims 35, 45, and 63, as well as the dependent claims are not rendered obvious by the cited combination. However, the examiner asserts that Pai by itself suggest the invention as claimed, and that by a substitution as suggested by Huang, the combination teaches the claims, even with the narrow interpretation of the appellant.

3. The rejection of independent claims 38, 48, and 66 is improper as the examiner failed to establish a prima facie case of obviousness.

The appellant argues that Huang fails to teach a shingle stack as defined by the instant specification. The appellant points to the instant specification page 14 line 10; "Shingle stacks are die stack wherein upper die may overhang die below them in a stack such that their centers are not aligned. The examiner points to Huang figure 2 for a die stack that reads on the above definition. The appellant argues that the structure of Huang cannot be fairly characterized as a die stack because it merely teaches a lead frame

with first and second die attached to it. However, the structure is two die stacked, thus it is a die stack (claim at least two die). The appellant argues that the die are adhered to a lead frame. However, the claims do not preclude the existence of a lead frame, interposer, or any other type of spacer.

The appellant argues that as above there is no reason to combine the two references, however, as above the examiner has asserted that there is reason to combine, the motivation being that the substitution is obvious and an improvement as to incorporating die of different sizes.

4. The rejection of independent claims 38, 48, and 66 is improper as the examiner failed to establish a prima facie case of obviousness.

The appellants argue that these claims are product by process limitations, as they recite "being curable at a first temperature" regarding the first adhesive and "being curable at a second temperature" regarding the second adhesive. The appellant argues that these are properties of the adhesives and not processing steps. However, as the stack is a finished structure, the curing of the adhesives is complete and the property is not of issue, therefore it represents a process step. Even if the limitations are considered to be properties of the finished product, the examiner points out that Pai teaches these limitations and that this is included into the rejection above. At best, this is a moot argument.

The appellant argues that the examiner has merely asserted that Pai anticipates the claims. However, attention is brought to Pai (column 3 lines 34-37) regarding this issue. The exothermic temperature is the temperature at which the adhesive loses its volatiles and cures. Pai anticipates this limitation.

B. Ground of rejection No. 2

1. The rejection of independent claims 68, 69, and 70 is improper as the examiner failed to establish a prima facie case of obviousness.

The appellants argue that Pai in view of Hakey fail to teach "wherein the stack comprises at least two semiconductor die" and "wherein each die in the stack of at least two die is successively thinner than the previous die". The appellant argues that although the die of Hakey are of different thicknesses, they are attached to the substrate rather than on top of each other. Hakey was not used to show the structure, but rather to teach that the stack of Pai would include different sized die. Pai teaches different types of die in the stack. Hakey teaches that the die types named by Pai are of different thicknesses. With two die of different thicknesses, one must be successively thinner than the other.

2. 3. The rejection of independent claim 68 is improper as the examiner failed to establish a prima facie case of obviousness.

The appellants argue that these claims are product by process limitations, as they recite "being curable at a first temperature" regarding the first adhesive and "being curable at a second temperature" regarding the second adhesive. The appellant argues that these are properties of the adhesives and not processing steps. However, as the stack is a finished structure, the curing of the adhesives is complete and the property is not of issue, therefore it represents a process step. Even if the limitations are considered to be properties of the finished product, the examiner points out that Pai teaches these limitations and that this is included into the rejection above. At best, this is a moot argument.

The appellant argues that the examiner has merely asserted that Pai anticipates the claims. However, attention is brought to Pai (column 3 lines 34-37) regarding this issue. The exothermic temperature is the temperature at which the adhesive loses its volatiles and cures. Pai anticipates this limitation.

(11) Related Proceeding(s) Appendix

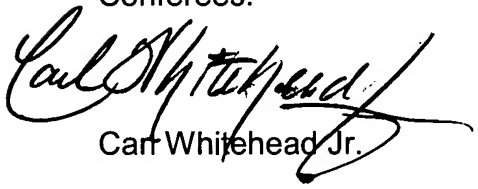
No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

David S. Blum

Conferees:



Carl Whitehead Jr.

Rickey L. Mack